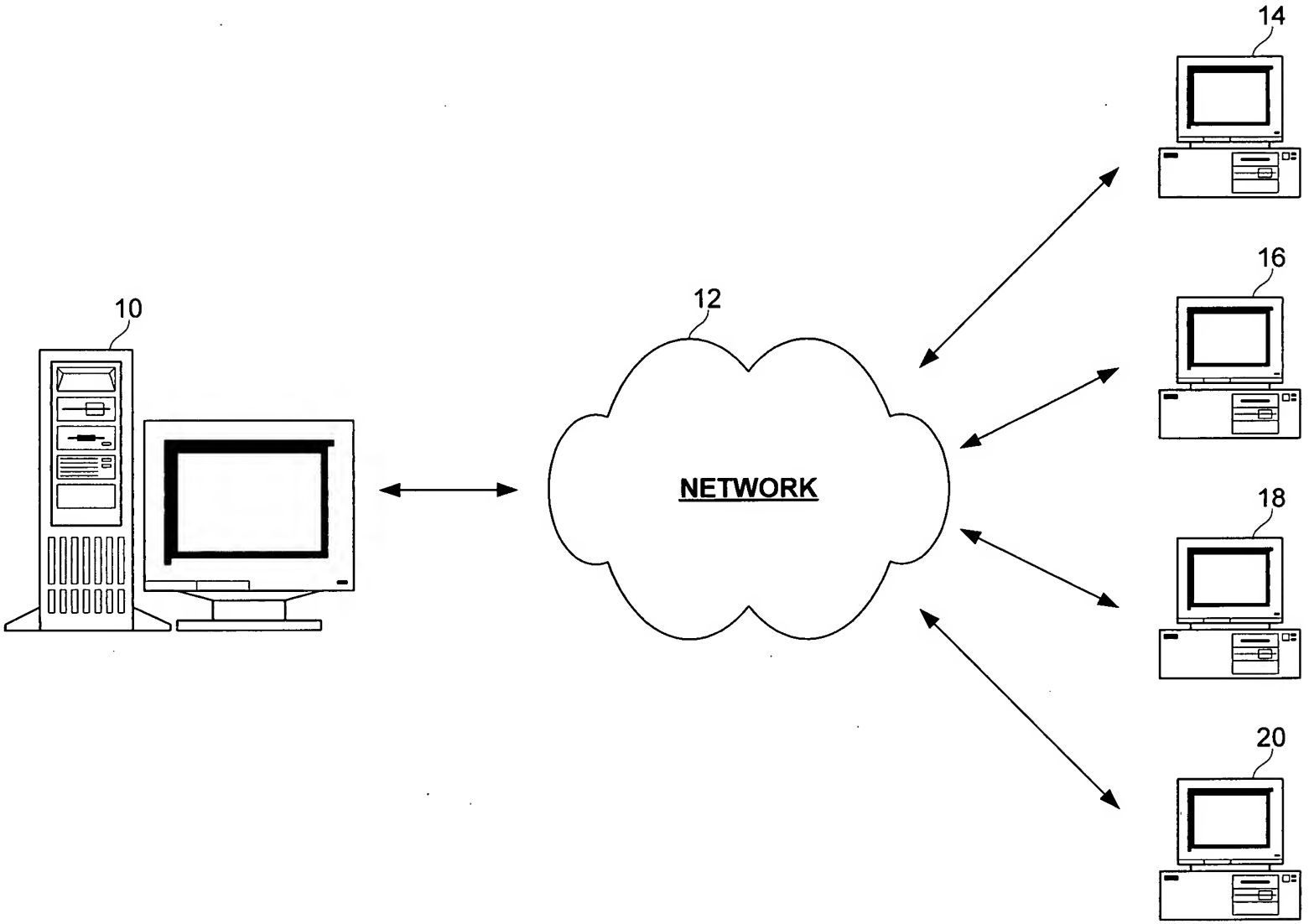

FIGURE 1

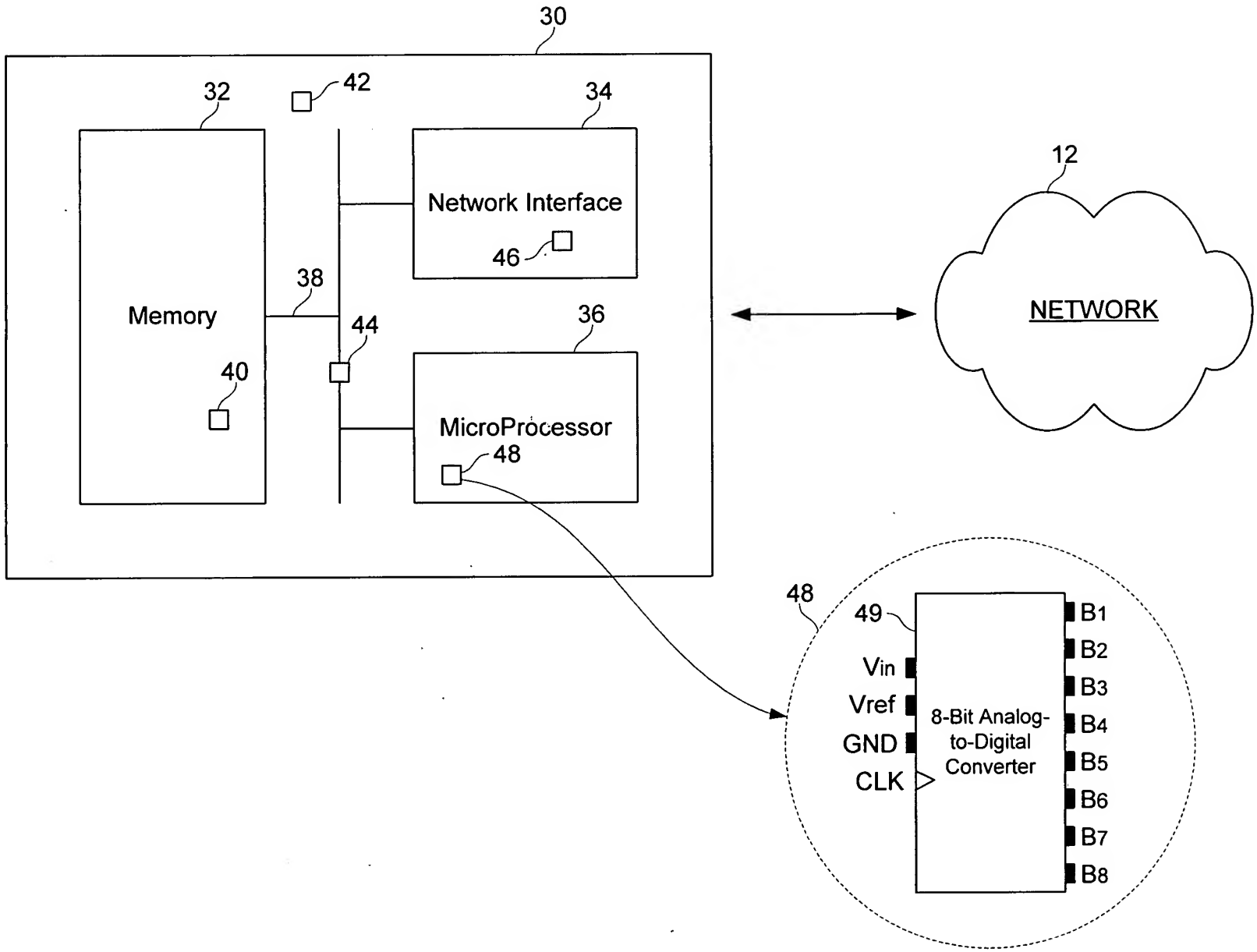
30
32
42
34
Memory
Network Interface
46
38
44
36
40
MicroProcessor
48
12
NETWORK
48
49
Vin
Vref
GND
CLK
8-Bit Analog-to-Digital Converter
B1
B2
B3
B4
B5
B6
B7
B8

FIGURE 2

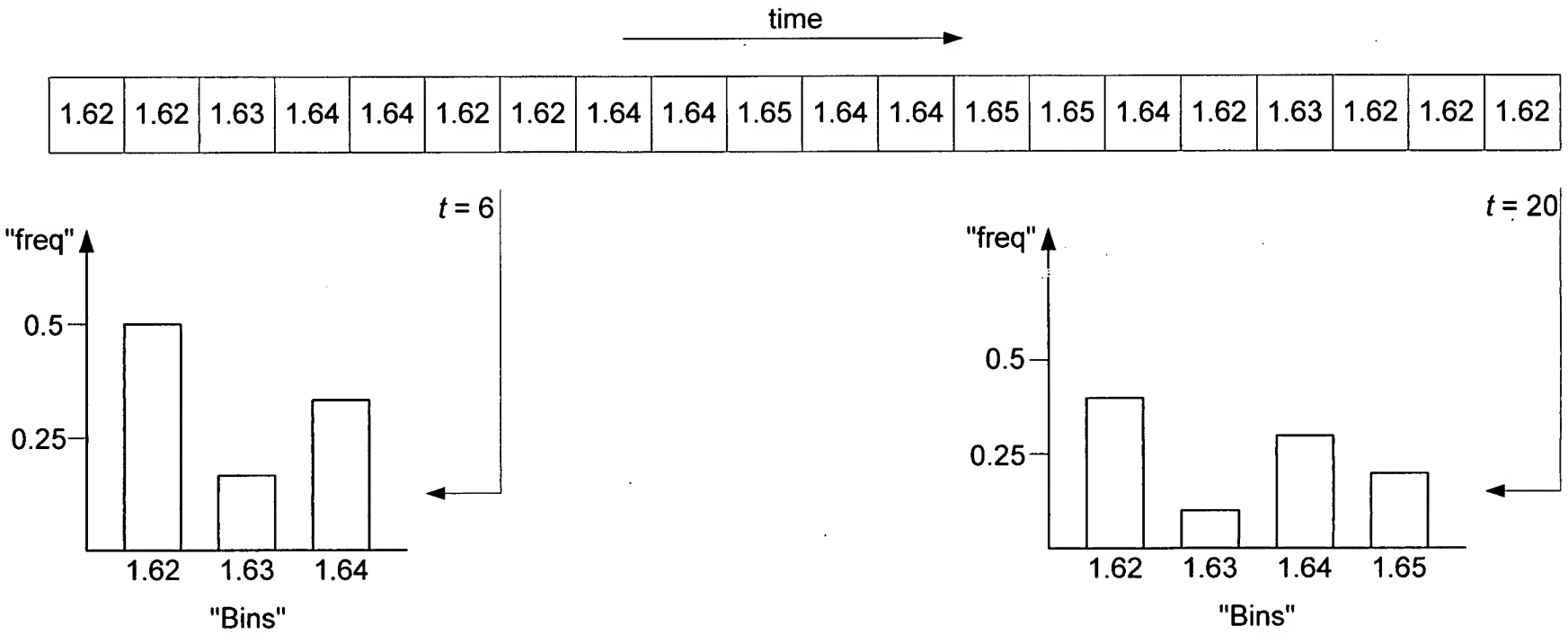
time
1.62 1.62 1.63 1.64 1.64 1.62 1.62 1.64 1.64 1.65 1.64 1.64 1.65 1.65 1.64 1.62 1.63 1.62 1.62 1.62
t = 6
"freq"
0.5
0.25
1.62 1.63 1.64
"Bins"
t = 20
"freq"
0.5
0.25
1.62 1.63 1.64 1.65
"Bins"

FIGURE 3

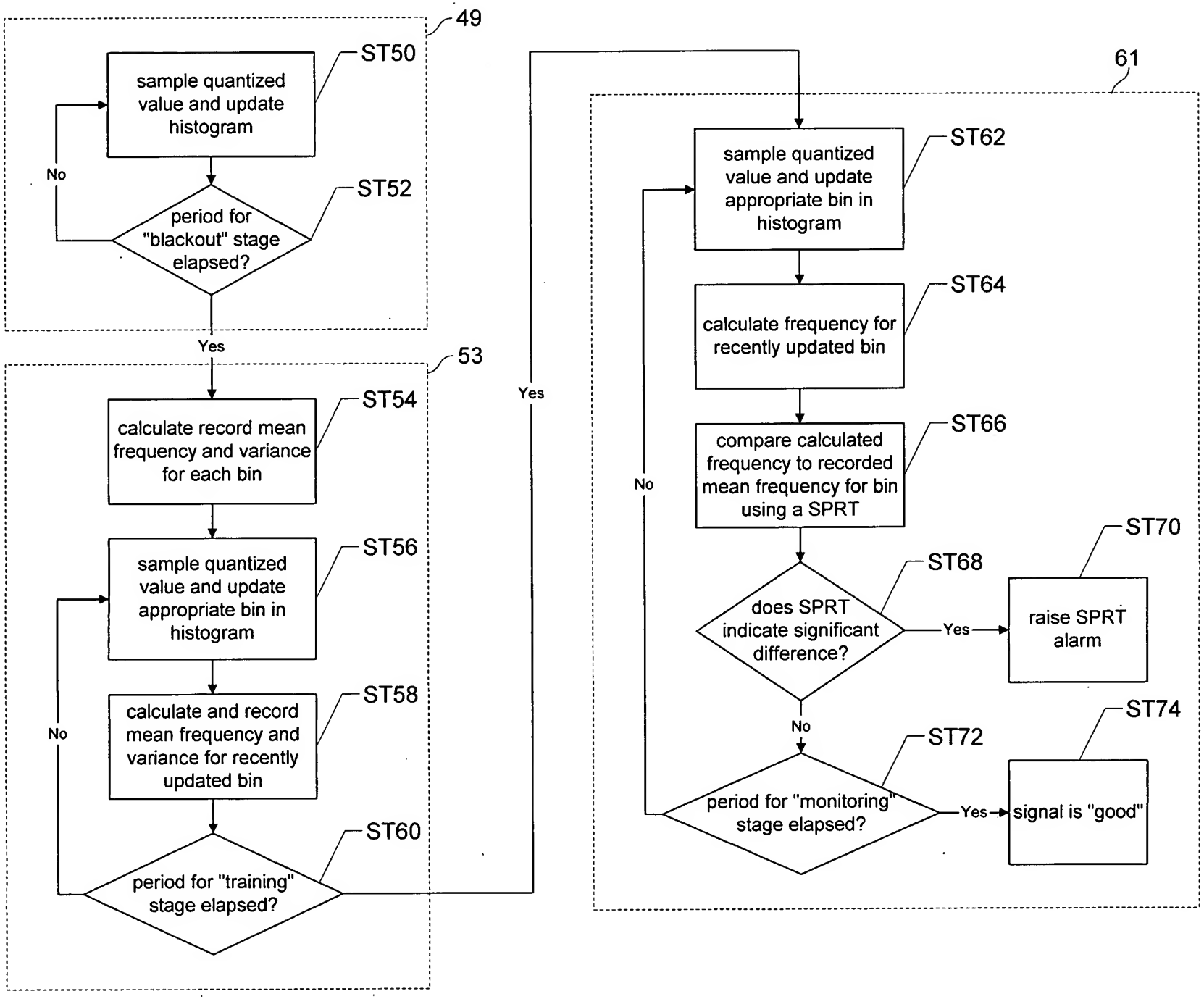
49
ST50
sample quantized value and update histogram
ST52
period for "blackout" stage elapsed?
No
Yes
53
ST54
calculate record mean frequency and variance for each bin
ST56
sample quantized value and update appropriate bin in histogram
ST58
calculate and record mean frequency and variance for recently updated bin
No
ST60
period for "training" stage elapsed?
Yes
61
ST62
sample quantized value and update appropriate bin in histogram
ST64
calculate frequency for recently updated bin
ST66
compare calculated frequency to recorded mean frequency for bin using a SPRT
No
ST68
does SPRT indicate significant difference?
Yes
ST70
raise SPRT alarm
No
ST72
period for "monitoring" stage elapsed?
Yes
ST74
signal is "good"

FIGURE 4